

Marathwada Mitramandal's
COLLEGE OF ENGINEERING

S.No.18, Plot No.5/3, Karvenagar, Pune-52

Accredited with "A++" Grade by NAAC | Recipient of "Best College Award 2019" by SPPU

Accredited by NBA (Mechanical Engg. & Electrical Engg.)

Recognized under section 2(f) and 12B of UGC Act 1956

Department of Electronics & Telecommunication Engineering

Activity: Flipped lab session

Class: BE II


Academic Year: 2023-2024

Course Name: VLSI Design and Technology

Topic: CMOS layout design for D Flip Flop

Dates: 16/10/23, 17/10/23, 18/10/23, 19/10/23

Details/Evidences/Photos:



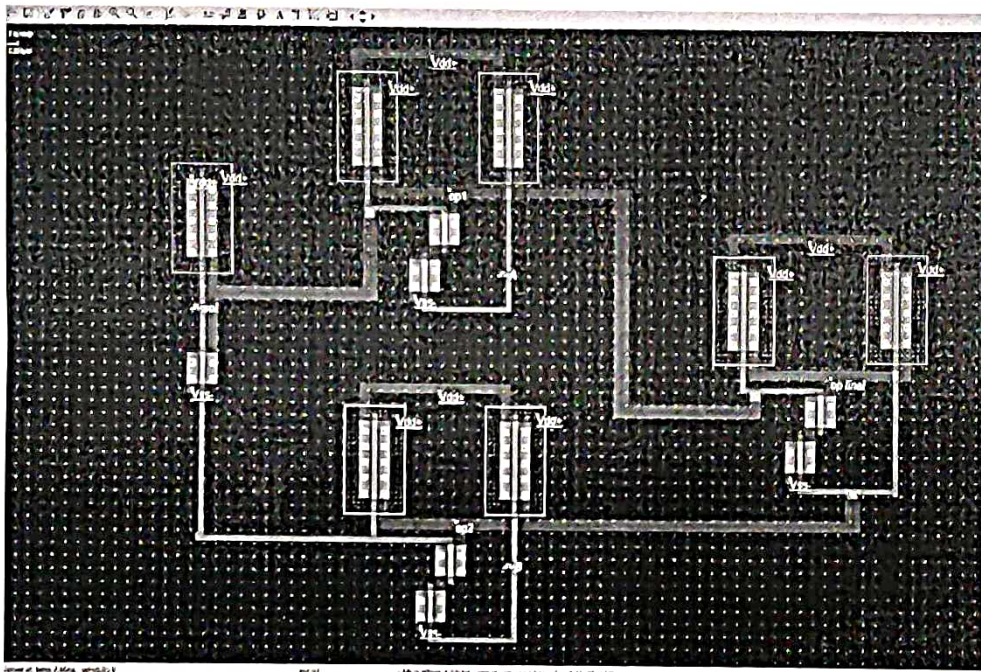
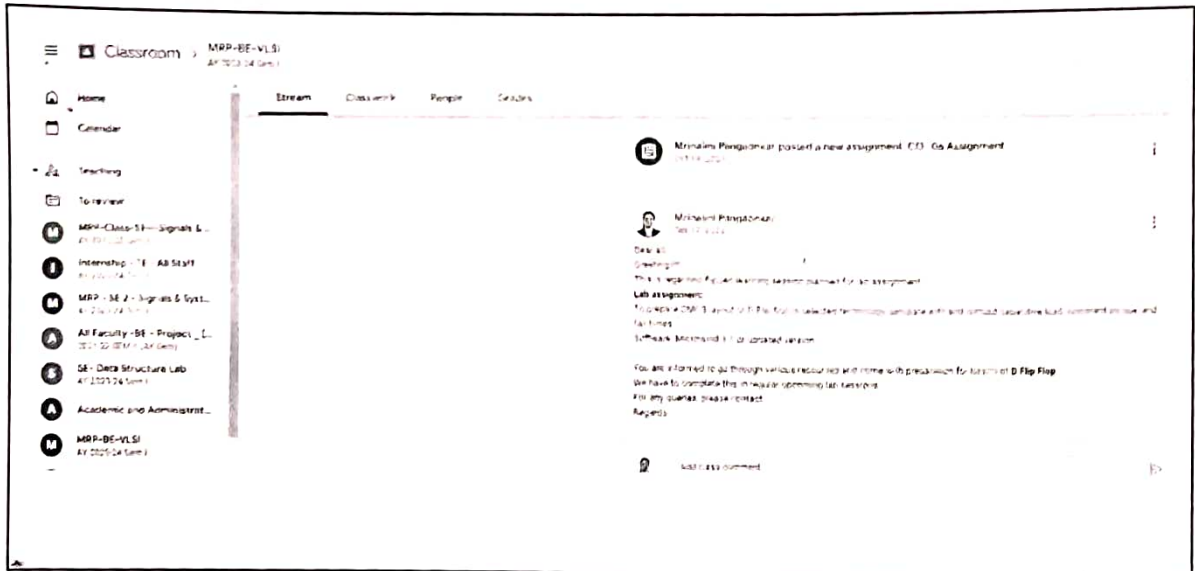
Mrinalini Pangoonkar
Oct 17, 2023

Dear all,
Greetings!!!

This is regarding flipped learning session planned for lab assignment.

Lab assignment:
To prepare CMOS layout of D Flip flop in selected technology, simulate with and without capacitive load, comment on rise, and fall times.
Software: Microwind 3.1 or updated version.

You are informed to go through various recourses and come with preparation for basics of **D Flip Flop**.
We have to complete this in regular upcoming lab sessions.
For any queries, please contact.
Regards



Ms.M.R.Pangaonkar *MPangaonkar*
Ms.H.N.Burande *HNB*
 Name & Sign of Course Coordinator


 Academic Coordinator